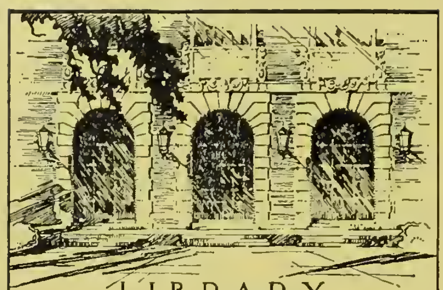

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REPORT NO. 91

DESIGN OF THE CORE STORAGE UNIT

by

S. R. Ray

August 20, 1959

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DESIGN OF THE CORE STORAGE UNIT

1. INTRODUCTORY REMARKS

It has been quite clear from the beginning of the computer organization studies in 1956 that the speed of the principal memory would be a major factor limiting the over-all computing speed. A considerable amount of effort during the early design period was therefore directed toward investigation of various memory organizations and types. Briefly, the major specifications which were imposed were that the memory contain 8192 registers of approximately 52 bits length capable of being randomly accessed in the minimum time feasible. Within the confines of the principal constraints such as speed of operation, availability of materials in production quantity, probable reliability of the final product, and economic factors, it was decided that the memory should be designed with standard toroidal ferrite cores organized according to the word arrangement[1] scheme, and having two cores per bit, operating in a partial switching mode with destructive readout. The words were to be driven by magnetic switches (one per word) which play the dual role of selection and transformation. A brief review of the reasons for these decisions is, perhaps, of interest. The decision to use standard ferrite cores is based, in part, on procurement, economics and on the fact that their characteristics are relatively well-known and controllable in manufacture.

The decision to use destructive readout is based on the fact that no non-destructive scheme, applicable to 8192-word memories or meeting the economic restrictions, was known.

The use of partial switching has its foundation in switching speed requirements. However, in order to maintain high reliability, the partial switching mode appears to require a higher degree of distinction between the "1" and "0" readout signals than would normally be obtained from a 1-core-per-bit arrangement. This high distinction (which might be termed large signal-to-noise ratio) is theoretically obtainable with the 2-core-per-bit system. In addition to the above, 2-cores-per-bit provides for switch-core loading which is virtually independent of the digit pattern, thereby reducing some annoying driver problems. The choice

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[1] Also called word-oriented, linear selection, end-fire or set-a-line method.

of the partial switching method is further based on both the fact that it reduces heating of the storage cores and that the volume of magnetic material in the switches is reduced which favorably affects the drivers.

All of the foregoing reasons for selecting the particular memory organization were considered to some degree at the outset. Experiments which have been performed since that time have shown the major outlines of the design to be quite sound. Considerable revision of details have, to be sure, been required. Probably the most serious objection to the 2-core-per-bit system is an economic one, not only in the sense that twice as many storage cores must be manufactured and wired, but also in the sense that twice as many digit drivers are required to operate a given number of bits.

2. GENERAL DESCRIPTION OF THE MEMORY

This section will describe, in broad terms, the presently proposed physical arrangement of the memory and the operation cycle.

2.1 Physical Arrangement and Basic Operation

The complete 8192-word memory is to be composed of two separate 4096-word memories. Each 4096-word memory includes 64 planes of storage cores having 64 words per plane. One magnetic switch is associated with each word as shown in Figure 1. The output winding (word or W-line) of the magnetic switch threads through a total of 104 storage cores arranged in 2 rows of 52 cores each. Two storage cores in vertical juxtaposition and served by a common W-line form the 2-core cell corresponding to one binary digit.

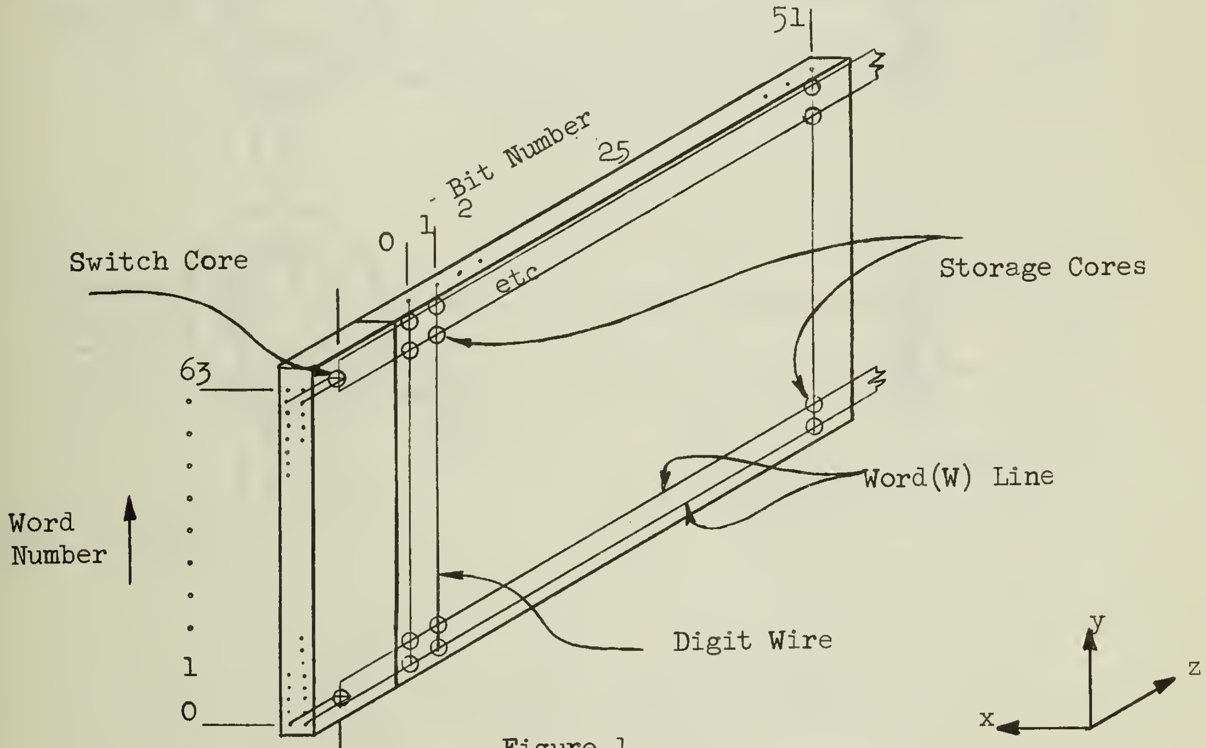

Figure 1
Single Core Plane (64 words)

The single wire per column threading through the storage cores is the "digit-sense" wire or, briefly, the digit wire.

A detailed diagram of switches with their respective words of storage cores is shown in Figure 2. Here, the four windings of the magnetic switch, X, Y, B (bias), and W (word-line) are shown. The magnetic field intensity produced by the continuous bias current holds the core material at the point indicated on the B-H diagram. Either I_x or I_y acting alone cancels the bias field while the other, if present, drives the core material into a high permeability region, R_1,

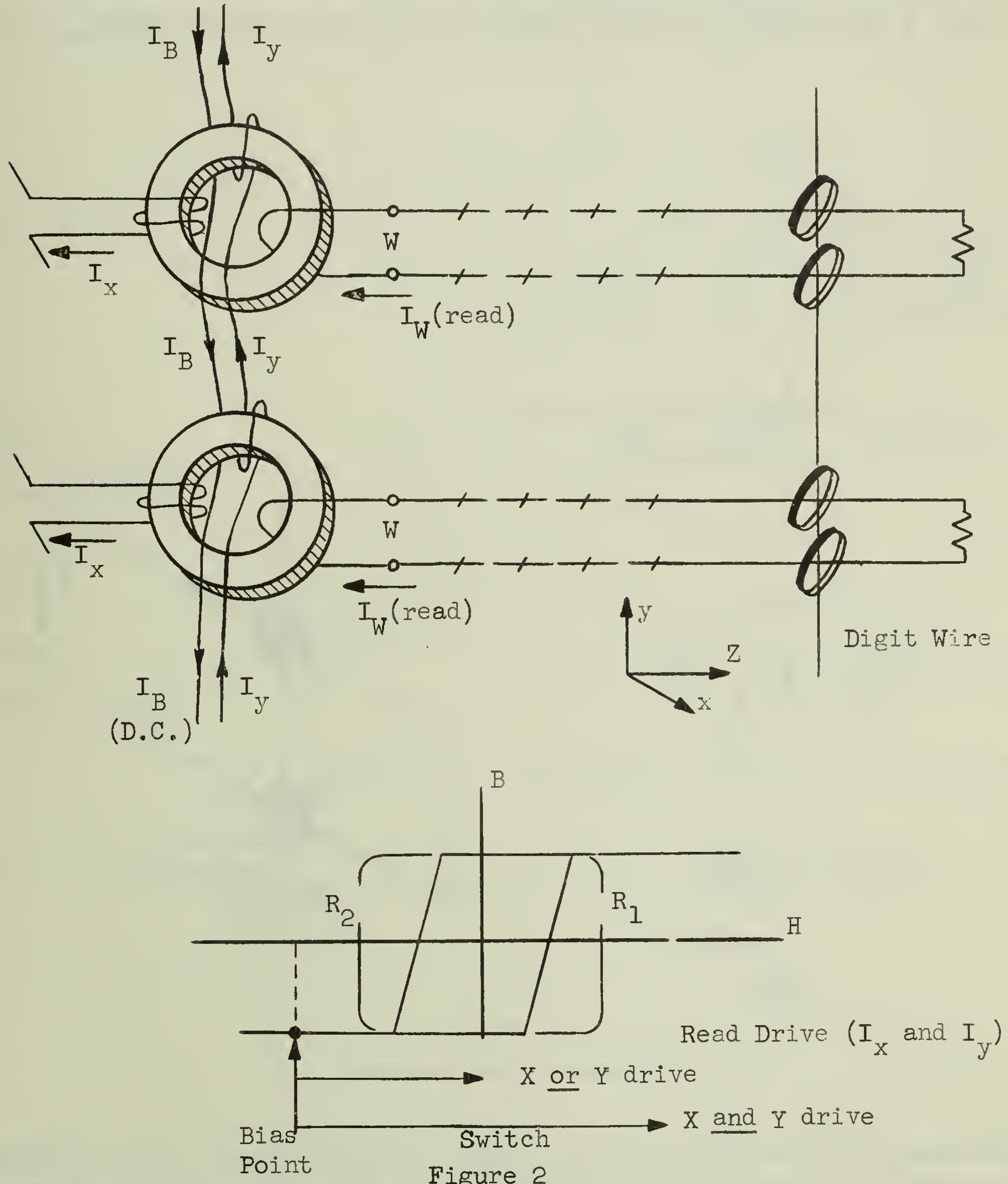

Figure 2

Detail of Switch Cores
(2 adjacent words in 1 plane)

where transformer action occurs.[2] The resulting W-line current is the "read current". Upon cut-off of I_x and I_y, the switch is driven back by the bias field through high permeability region R_2, where transformer action again occurs producing a W-line current called the "W-line write current" having opposite polarity to that of the read current.

The operation of the storage cores proceeds as follows. Referring to Figure 3, we assume that binary "0" is represented by core N containing $-B_r$ flux density while core P contains $+B_r$.[3] Assigning the convention that read current produces positive field intensity, the application and removal of H (read) will,

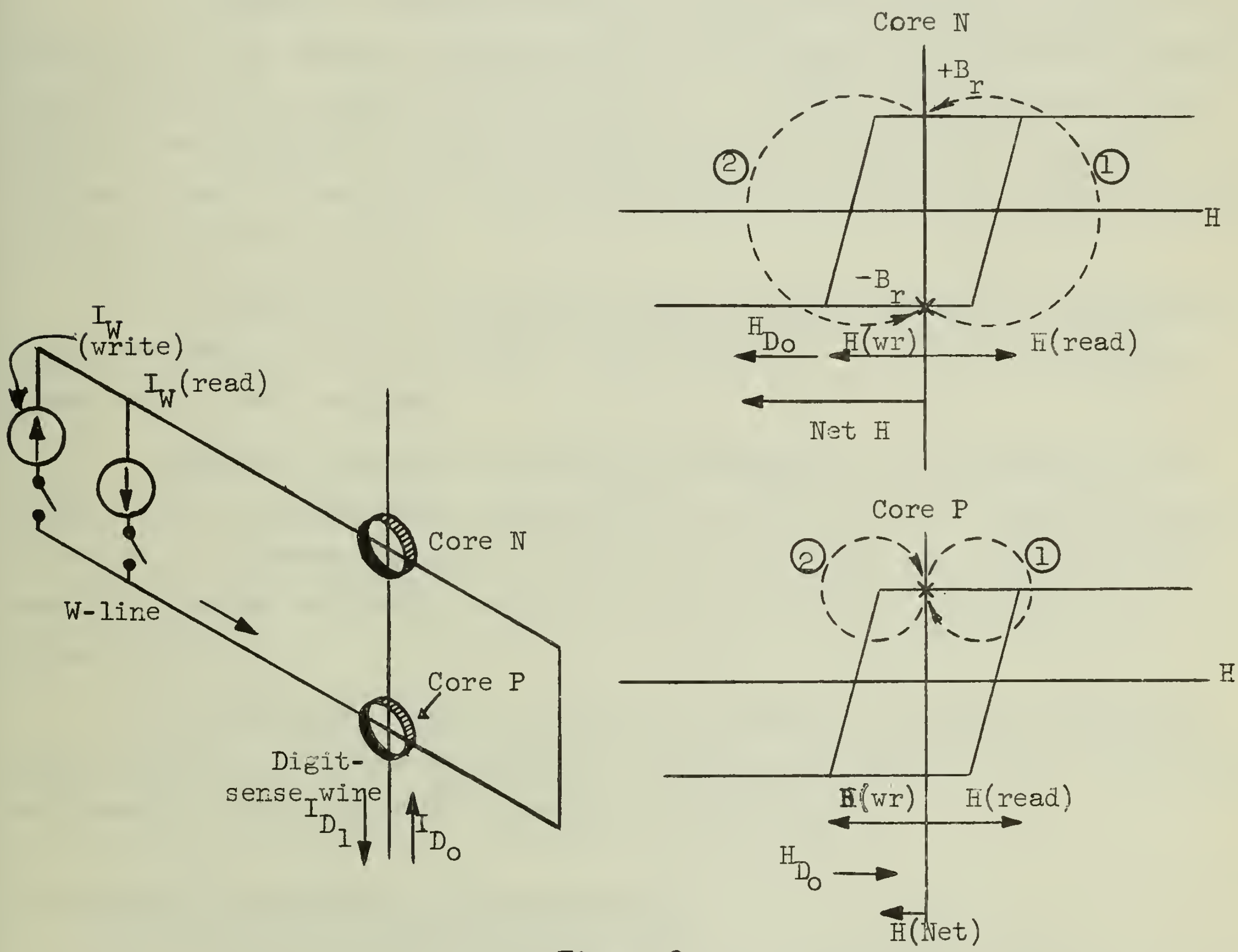

Figure 3

Storage Core Operation

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[2] The B-H loop is used loosely in this section for descriptive purposes and should not be considered completely applicable in actual circumstances.

[3] This description will be amended slightly in Section 2.3.

given sufficient time, cause the magnetization of core N to move from $-B_r$ to $+B_r$ along path 1. Careful examination will show that the resulting voltage pulse developed across the ends of the digit-sense wire is the difference between the large change of flux in core N and the small change from core P. If it is now desired to rewrite the digit previously stored, then both cores must be placed in their original magnetic states. This can be done by applying I (write) in the W-line and I_{D_0} in the digit line. Under the assumed convention, the resultant magnetic field intensities in the two cores will be H (net) as indicated which causes the magnetization of the cores to follow path 2 indicated on the diagram, achieving the desired end.

If binary "1" had been stored, we would have, initially, core N at $+B_r$ and core P at $-B_r$ which, upon application of I (read), would produce an output (sense) pulse of reverse polarity to the "0". In fact, the production of bi-polarity sense signals is a major advantage of the 2-core-per-bit system. Rewriting of the "1" proceeds in the same manner as rewriting "0" except that I_{D_1} is applied instead of I_{D_0}.

It should also be noted that after the read operation, both cores of a bit are always in the $+B_r$ state so that either "1" or "0" can be written, regardless of what was read.

Figure 4 indicates the physical arrangement of the magnetics, the drivers, and the sense signal preamplifiers for one-half of a 4096-word memory. It should be observed that each X driver or Y driver serves 32 switches while each digit driver and sense preamplifier serves one bit of the 2048 words on the planes indicated.

The remaining half of the 4096-word memory is exactly like the one shown. The pair of sense preamplifiers associated with, say, bit "i" in the two half memories then feed into a common sense amplifier.

2.2 General Description of the Memory Cycle

The block diagram of the memory unit is indicated in Figure 5. It is assumed that the address of the word to be accessed arrives at the memory prior to or simultaneously with the memory request signal. The latter sets the memory cycle flipflop which starts the memory cycle timer and the X-Y timer.

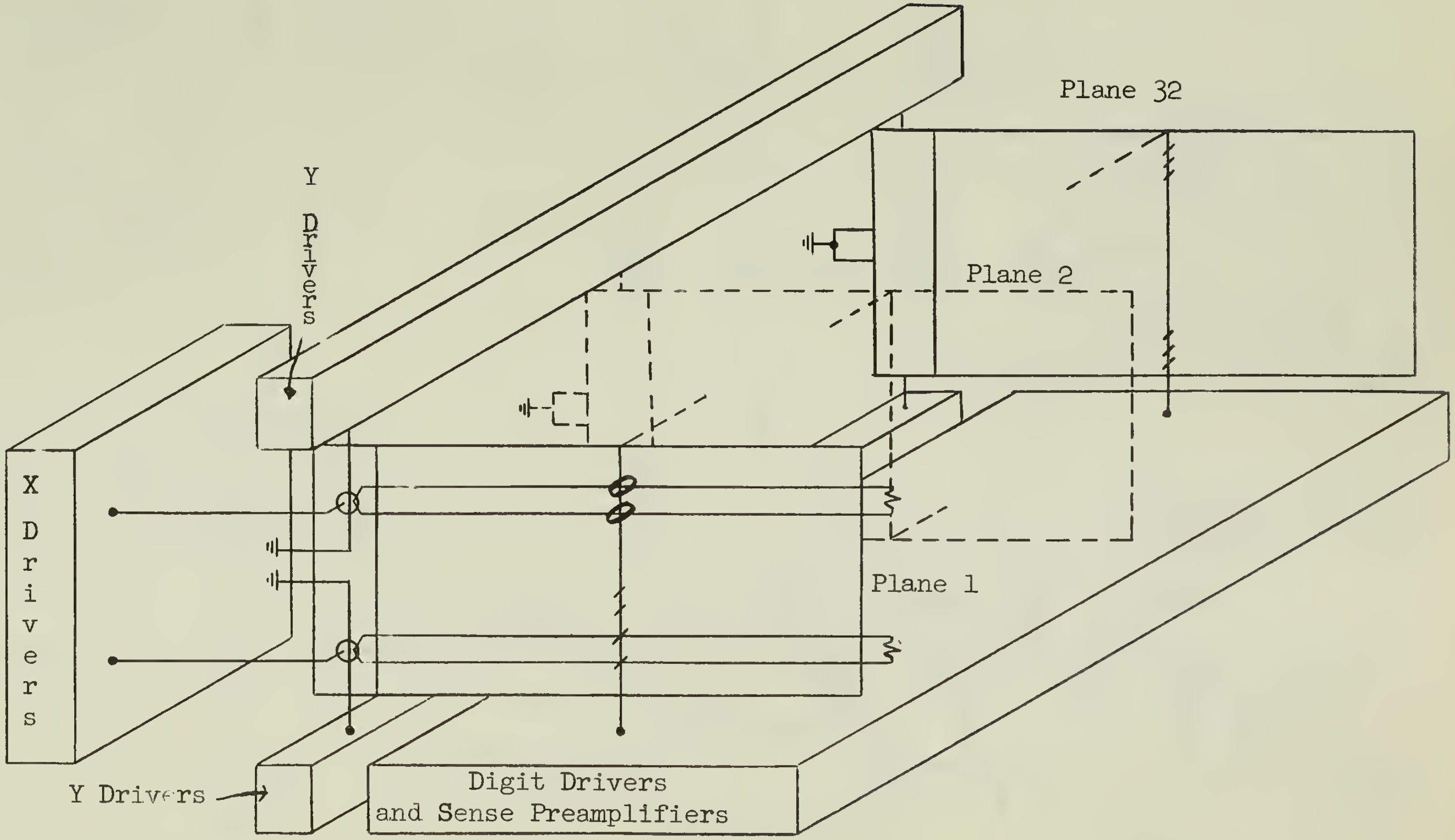


Figure 4

Physical Arrangement of Memory

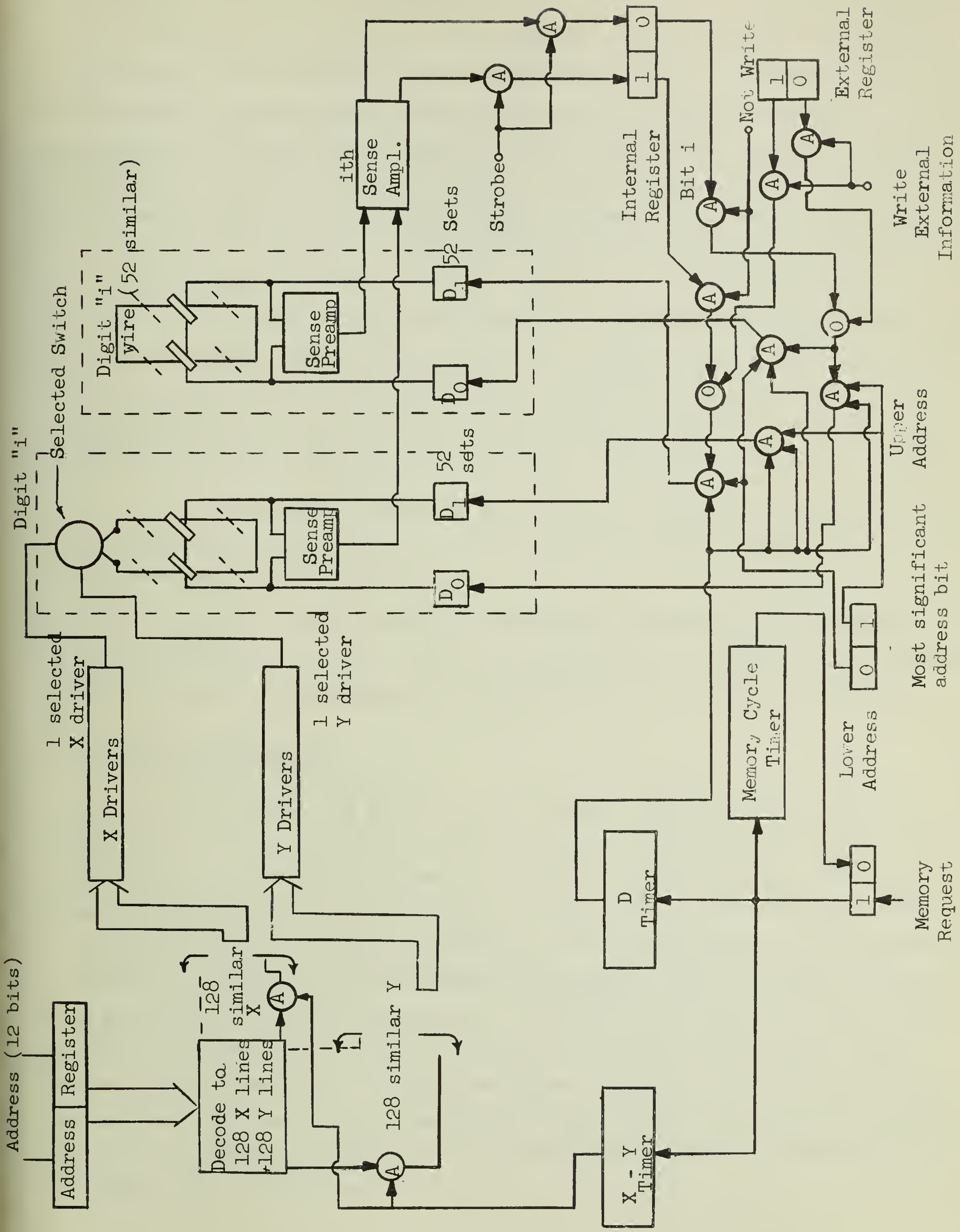


Figure 5

Memory Block Diagram

The X-Y timer output travels through the path allowed by the decode logic turning on one X driver and one Y driver. The magnetic switch thus selected delivers read current into the W-line, which reverses the flux in one storage core of each pair sending 52 sense signals simultaneously down the digit-sense wires. After the signals are amplified to standard logical levels, they feed into flipflops through gates controlled by the gate or "strobe" signal which, when turned off, blocks noise signals to the flipflop input. Assuming we wish to rewrite the word just obtained, the flipflops in which the word is stored determine which half of each digit driver, D_0 or D_1, is to be turned on. The turn-on is further controlled by the D timer. At approximately the same time that the D drivers (one per digit) turn on, the X-Y timer turns off causing the X-Y drivers to turn off and the switch core of the selected word to produce the W-line write current which coincides with the 52 digit currents and resets the desired word. After turn-off of the digit drivers and the memory cycle timer, the cycle is complete.

If it had been required to write a new word in place of the one read out, the lines carrying the new information could simply be substituted for the lines from the internal register.

The full write and partial substitution operations may be seen to proceed by ignoring all or part of the information read into the internal register and substituting the complementary information from the external register.

2.3 Partial Switching

For a given core material and driving field, the time required to switch from a certain initial to final state of flux remanence is roughly proportional to the difference between the initial and final states. Thus, in Figure 3, if binary "0" is represented by core P at $+B_r$, the core N will need to switch only half as "far" as previously. This arrangement is called partial switching, in this case, 50% switching (as opposed to full or 100% switching in the originally described arrangement). In partial switching, the sense signal from core N decreases with the percentage of switching. Since much higher reliability is possible in recognizing signal polarity than in discriminating between two amplitude ranges, the present arrangement provides both the speed advantage of partial switching and the more reliable polarity discrimination for the small signal amplitudes.

3. DETAILED ENGINEERING CONSIDERATIONS

This section will deal in detail with various problems and effects which have been encountered in the memory design studies up to the present time.

The non-standard equipment which has been employed in the tests is as follows:

1 complete core plane (64 words),

2048 simulated 3-bit words having the form of a 3-bit wide section cut out, as it were, of 32 stacked core planes,

3 X-Y drivers,

6 digit drivers,

various pulse programming units, additional switch and storage cores.

3.1 Digit Lines, Digit Drivers and Sense (Readout) Signals

3.1.1 Digit Line Propagation Time

It was originally intended that each of the digit lines be composed of a 3-wire group (the digit-sense group), thereby allowing a separate wire for each of the 3 functions, set 0, set 1, and sense. Subsequent investigation showed that the delays indicated in Table 1 exist for various numbers of wires in the digit-sense group.

Table 1

No. of wires in digit-sense group	T
3	220 mμs
2	180 mμs
1	75 mμs

(T = transmission time of the signal down a wire threading 4096 bit cores, each wire being approximately 27 ft. long.)

When more than one wire composes the digit-sense group, it is found that the mutual coupling coefficient between wires in the group approaches unity for only a few feet of wire by reason of the ferrite surrounding them commonly.

It is also clear that the wire-to-wire capacitance approaches the maximum possible for the wire size and length. These factors account for the relatively slow propagation of signals in the case of multiple wires.

3.1.2 Digit Line Oscillations

An effect of much greater importance than the propagation time itself can be explained by considering two parallel wires coupled tightly, both inductively and capacitively, as in Figure 6. One wire may be considered to be a digit driver wire, the other a sense wire. Also assume that the resistances at the ends of the lines are such that they absorb all incident energy on the wire i.e., the lines are individually terminated in their characteristic impedances. Upon application of a step of voltage, E, at x = 0 on wire A, a wave front propagates to the right on line A, inducing a current in wire B until it arrives at x = d. However a considerable amount of energy has been transferred into wire B (by the assumption of tight coupling) which propagates both to the right and left. Thus the signal propagating to the left on wire B after the arrival of the original wave front at x = d, continues to transfer energy back into wire A, etc. Briefly, the wave energy transfers back and forth between the storage elements of wires A and B until it is dissipated in wire and termination resistances.

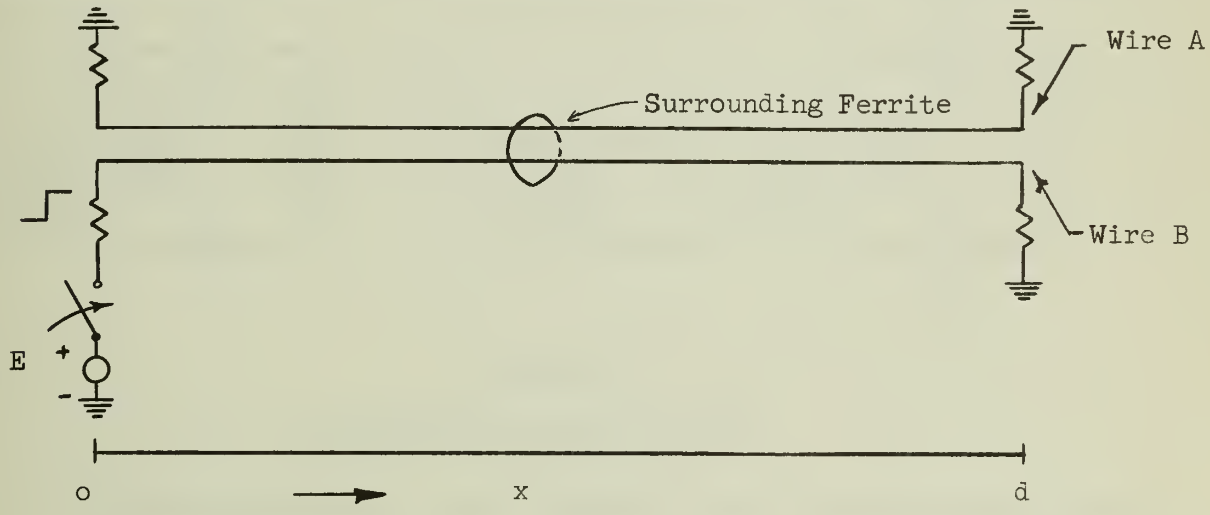


Figure 6

Two Wires of a Single Digit-Sense Group
(threading through common storage cores)

The damping rate of this oscillatory system was found to be intolerably slow, requiring about 1 μs to settle below the level of the sense signal.

3.1.3 Digit Line Drive

After study of these problems, it was decided that the most expeditious solution was to use a 1-wire digit-sense group. The method of producing the bi-directional current drive is indicated in Figure 7.

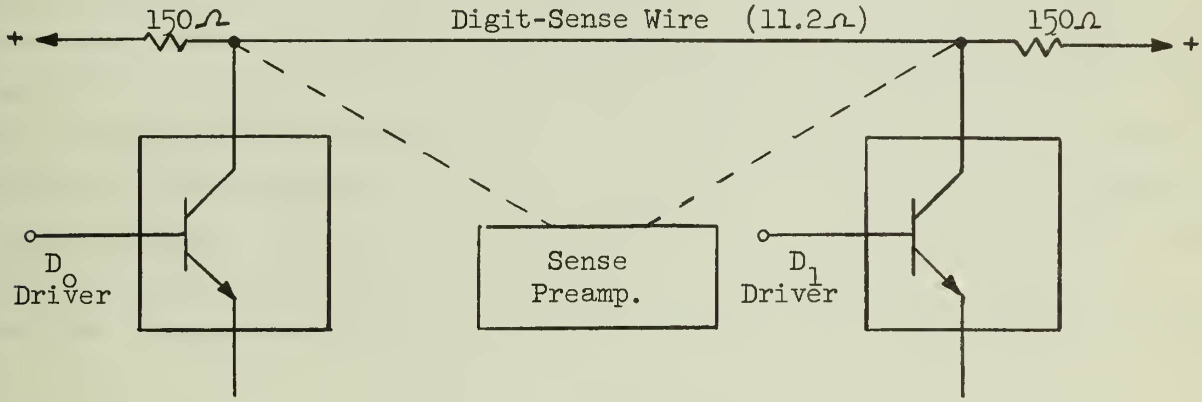


Figure 7

Arrangement of Digit Drivers

It can be seen that in this situation, the digit drivers, D_0 and D_1, must provide somewhat more than twice as much current as required to flow through the wire. The driver current in our case is 520 ma nominal. Because of the transistors available, it is scarcely more difficult or expensive to supply 520 ma than the 250 ma which would be required with separate wires for the digit drivers.

Experimental tests of the 1-wire system of Figure 7 indicate that the oscillations encountered in a multi-wire system have been eliminated.

3.1.4 Sense Signal Interference

Another problem which was encountered in the design process was that of mutual interference of sense signals. Each digit-sense wire is rather well shielded from the others, magnetically, by the storage cores. However, it can

be shown that the total capacitance existing between a given digit-sense wire and all others is of the order of several thousand micromicrofarads. If the rise time of a sense signal is comparable to or shorter than the propagation time down the digit-sense wire, then there will be a strong mutual interference of sense signals which is dependent on digit pattern.

Figure 8 indicates the shape which "fast" sense signals might take at a certain time as a function of position on the digit-sense wire. It will be apparent that in case, for example, the word 111···101···111 is read, the "0" would suffer severe attenuation. If, however, the sense signal rise time is long compared to the time delay of the digit-sense wire, then the only effect of sense signals will be to move the potential of the whole wire relative to the common reference without substantially affecting the potential difference developed across the ends of a wire by a sense signal. The latter statement is a description of the "common-mode effect" wherein the digit-sense wires may be considered as lumped, rather than distributed, elements. It is believed that the conditions under which

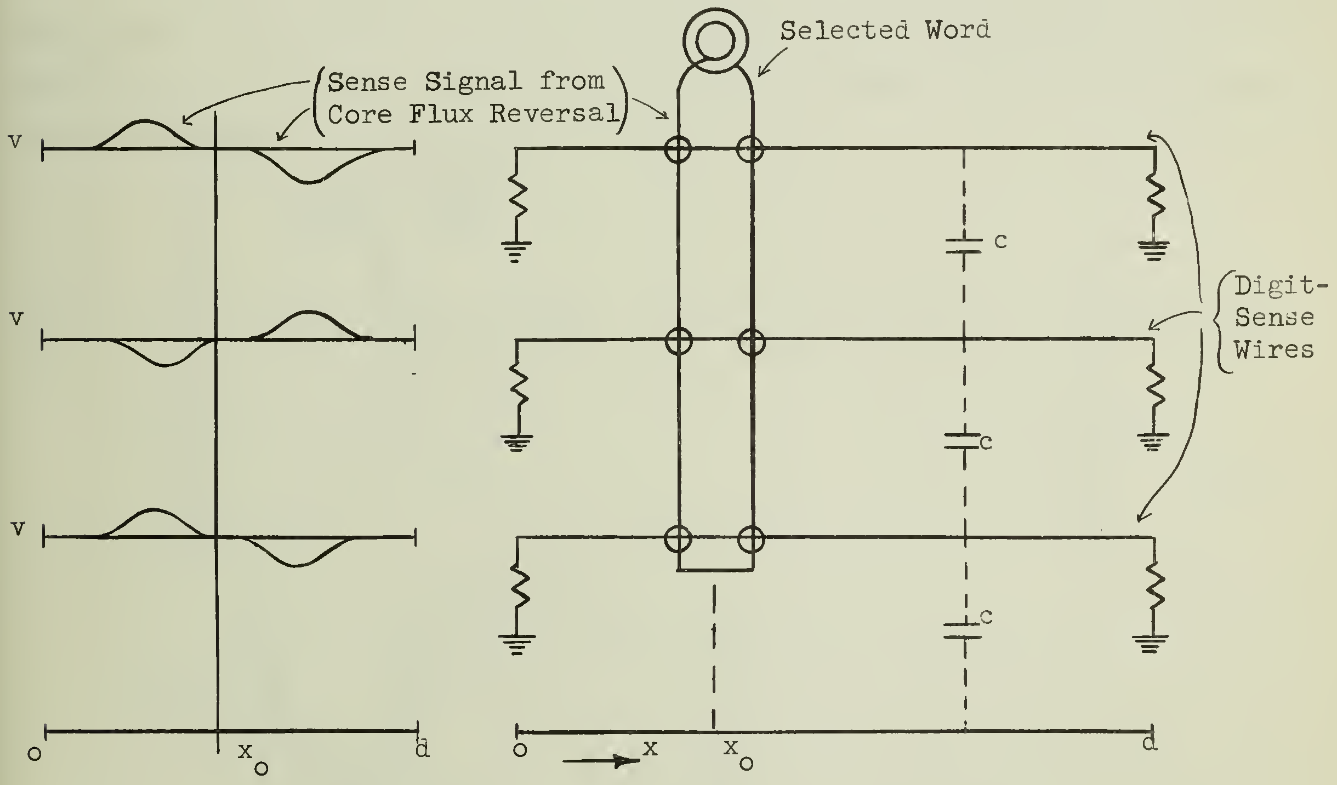


Figure 8
Interference of Sense Signals

advantage may be taken of the common-mode effect have not been spelled out very clearly in the past. It has been a factor in the present design and will undoubtedly require consideration in other fast memories in the future.

In particular, it has been necessary to reduce the length of digit wires in the present memory to about 75 mμs delay as compared to the sense signal rise time of about 150 mμs. Whether this is entirely adequate is not yet known. Thus, at present, each digit wire threads through 4096 storage cores (2048 words), there being, therefore, 4 distinct digit wires for each binary digit of all words, two digit drivers (D_0 and D_1) associated with each digit wire and one sense preamplifier for each digit wire. Thus, the total for a 52-bit computer word comes to:

2 x 52 x 4 = 416 D_0 and D_1 drivers
1 x 52 x 4 = 208 sense preamplifiers

3.1.5 Digit Drive Reaction

Another important effect which has not yet been considered is called the "digit drive reaction". The effect is observed in the following way: if we operate one of the digit drivers, e.g., D_0 as in Figure 9, the resulting waveforms are as indicated.

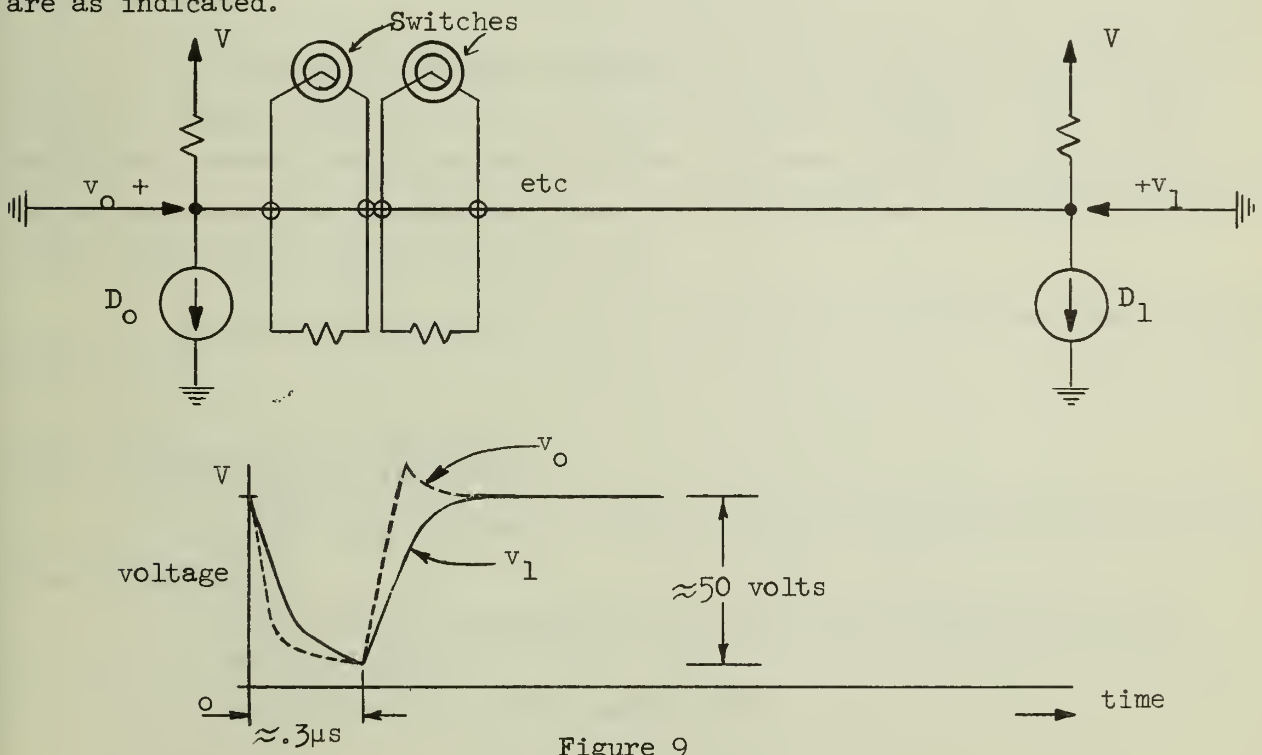


Figure 9
Digit Drive Reaction

The difference voltage $v_0 - v_1$, which is sustained for some time after turn-off of the digit driver, is called "digit drive reaction". It is immediately seen that this resembles the reaction of an inductor to current turn-off. This, in fact, appears to be a possible explanation, the inductance being that of the digit line. It may also be explained as the mismatch of a lossy transmission line.

In any case, the effect of digit drive reaction on memory cycle time is very important, because the voltage difference across the digit wire is applied to the input of the sense amplifier which may therefore be blocked for as long as 1.4 µs.

Several solutions to this problem appear promising but have not yet been experimentally investigated.

3.2 X-Y Drive

The problem of deciding precisely what characteristics the read-write drive should have is quite complex. A multitude of schemes have been proposed in order to attain the various goals of economy, adaptation to available transistors, large drive current, and a host of other more of less desirable characteristics.

For the memory design requirements of our case, the only immediately practical driver elements, which have been available throughout most of the development period, have been vacuum tubes. However, adequate transistors have become available (in experimental lots) in recent months. Therefore the transition to transistor drivers has been made.

The way in which the transistor drivers are applied has been indicated in Section 2 .

3.2.1 Current Rise in X-Y Lines

In mechanizing the chosen method, several difficulties are encountered, some of which are:

1) the problem of bringing the X and Y line currents up to full value rapidly,
2) switch core efficiency and heating.

The first problem can be explained by considering a series-connected group of switch core primaries as a lumped inductance. This is, in fact, a very good approximation to the observed effect. Therefore, according to Figure 10, we initially have a situation equivalent to switching a voltage generator, V, across an inductor, L, in which case the current in the inductor, i_L, rises linearly with time according to the formula, $i_L = \frac{V \cdot t}{L}$. In the mode of operation used, the voltage V is limited to $V < 1/2 v_{cb}$, where v_{cb} is the maximum reverse rating of the transistor, the factor 1/2 being required by the voltage reversal across L when transistor T_1 is cut off. Thus, if $V = 30v$, $i_L = 750$ ma., $t = 125$ mμs, we have $L = \frac{30 \cdot 125 \cdot 10^{-9}}{0.75} = 5$ μh. The inductance of switch core primaries may thus be measured and along with other factors, one eventually arrives at a compromise set of values for the number of turns on a switch core primary, the primary current, rise time, etc.

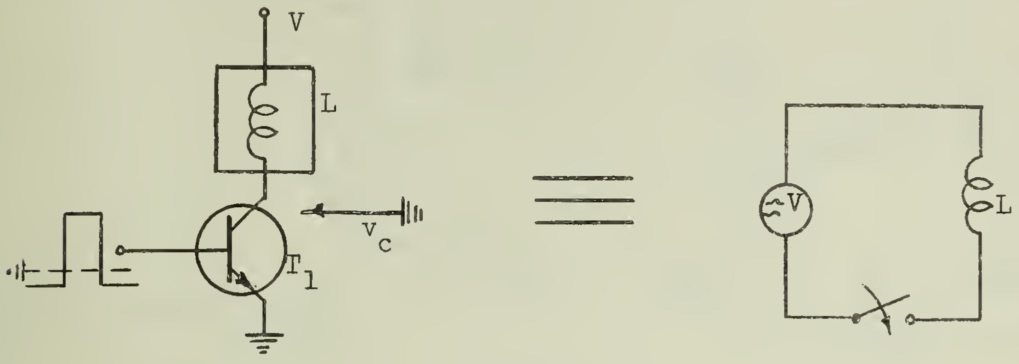


Figure 10

Equivalent X or Y Line During Initial Current Rise

3.2.2 Droop Network

It is possible to obtain faster rise time for a given v_{cb}, i_L, and L than indicated above by taking advantage of the fact that the voltage drop across the switch peaks initially and then drops as the flux becomes exhausted. This is indicated in Figure 11 where a transistor having a maximum v_{cb} rev. of 75v is assumed. It can be seen that the voltage, v_s, droops while the driver transistor is conducting.

With this simple arrangement, it is possible to apply about 45v (as opposed to 30v otherwise) across the switch cores initially and therefore either

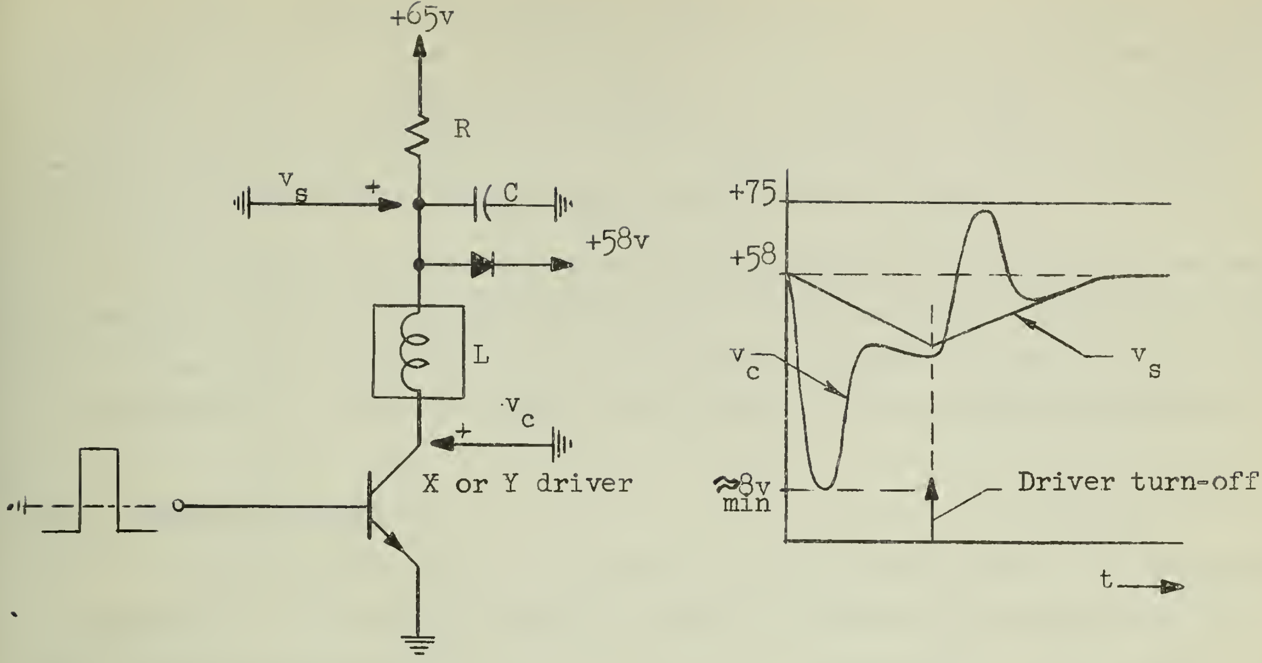


Figure 11

Application of a "Droop" Network

bring the current up to full read drive faster by the factor 1.5, use 1.5 times as many switch cores in series, or obtain a combination of several other desirable effects. It will also be noted that driver power dissipation is reduced.

In this way, it is possible to operate in the following regime:

Number of switches in series/driver = 32
Switch Core Turns: X = 2
Y = 2
Bias = 1
W-line = 1

Line inductance for 32 primaries in series = 4.5 μh; voltage applied across load (32 primaries), ≥ 45v; nominal current in X and Y lines I_x and I_y = 840 ma; rise time of I_x and I_y = 85 mμs (with step-voltage applied).

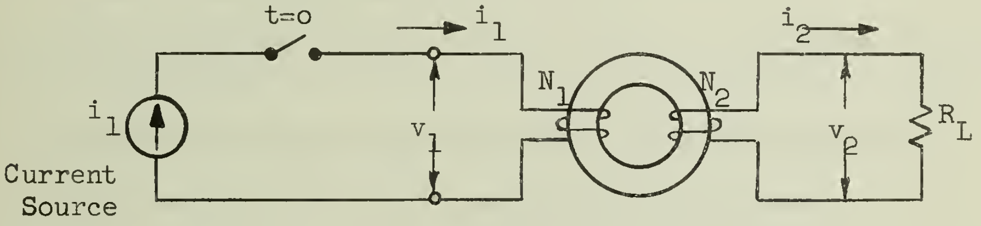
With transistor type 2N1072 (Western Electric) it is possible to apply the voltage "step" in about 50 mμs which, of course, increases the time required for the X or Y line currents to rise relative to the above figure. The total time required from the application of the drive signal on the base of the output transistor until the word line current peaks is about 175 mμs.

It should also be noted here that the bias line turns must be as small as possible in order to minimize the transfer of energy into the bias line, and therefore minimize the oscillation of the lines. Further reasons for this particular choice of switch core turns will be given in the succeeding material.

3.2.3 Switch Core Heating

The matter of switch core efficiency and heating have been considered in some detail. It has been found that free air surface temperature rise of the switches operating at 667 mc (1.5 μs cycle) is about $90^{\circ}C$. The effect of a blast of air at room temperature from a small fan is to reduce the surface temperature rise to the range 20 to $25^{\circ}C$. Whatever the corresponding condition inside the ferrite is, the effect of the heating (with air blast) on over-all memory operation is quite tolerable.

A heating measurement was made under the conditions indicated in Figure 12. After graphically recording v_1 and v_2, the energy loss to the core per half-cycle, $\int_{0}^{T}(v_1 i_1 - v_2 i_2)dt$, was found to be 0.87 μjoule. This energy is given to the core $1.33 \cdot 10^6$ times per second for a cycle time of 1.5 μs. Therefore, the power dissipation, $P = (1.33 \cdot 10^6) \cdot (.87 \cdot 10^{-6}) = 1.16w$ corresponded to approximately $90^{\circ}C$ surface temperature rise in free air.



N_1 = 4 turns; N_2 = 2 turns; I_1 = 550 ma; $R_L = 9.72\ \Omega$

Figure 12

Switch Core Heating Test

3.2.4 Decay of Word-Line Current

For W-line currents below the storage core threshold, it can be seen that a W-line may be represented by a linear inducatance paralleled by a resistor. The resistance of the W-line itself is 0.5 Ω while the effective inductance is approximately 0.5 μh. It is desirable to obtain the smallest possible W-line time constant in order to avoid possible additions of disturbance signals. On the other hand, the W-line resistance must be as small as possible from the viewpoint of X-Y drivers and switch efficiency. The addition of 1.5Ω in series has been found experimentally to be a reasonable compromise. Thus, the time constant of the W-line can be reduced to 0.25 μs. It can be shown that for this condition, the current flowing in a disturbed W-line cannot exceed the storage core threshold.

3.3 Choice of Magnetic Materials

Switch cores and storage cores were chosen to provide, as well as possible, the following properties which were considered desirable.

3.3.1 Switch Cores

1) Square-loop material to provide selection,
2) Circumference-to-volume ratio as small as possible,
3) H_0 small,
4) Good squareness,
5) High Curie temperature,
6) Total flux equal to 1/2 the flux required to fully switch one storage core per bit,
7) Aperture large enough to admit the required cross-section of winding.

A ferrite was chosen which has the following properties:

Electrical: $B_s = 2100$ gauss, $B_r = 2000$ gauss

$H_0 = .55$ oer.

$T_c = 190°C$

Example: RCA 222M2

$$R_s = .88 = \frac{B(-\frac{H_m}{2})}{B(H_m)}$$

Physical Dimensions: O.D. = .08"
I.D. = .05"
Height = .025" per core

The switch is composed of 12 of the cores stacked as a tube.

Upon switching, the switch material flux density changes by about 4100 gauss, so that a total flux of 1.2 μwebers is delivered by the switch to the storage cores.

3.3.2 Storage Core Material

The storage cores were chosen for the characteristics:

1) Small switching constant,
2) Moderately low H_0
3) Small size (i.e., large H for given drive mmf),
4) Low cost,
5) High Curie temperature,
6) Good squareness,
7) Good flux density.

Ferrite must be chosen because of economic considerations. Since small switching constant and low H_0 are incompatible, it is clear that H_0 must be chosen as large as possible considering the maximum drive currents which can conveniently be supplied. The choice of relatively large H_0 also provides better tolerance to switch core disturbances along with high Curie temperatures, squareness, and flux density.

The storage cores which were chosen under these conditions have characteristics as follows:

Electrical: B_s = 2000 gauss Example: RCA 3018H
H_0 = 1.2 oer.
S_w = .6 oer-μs
Flux for half-switching of 52 cores = 1.03 μwebers
For 750 ma-t net applied drive:
Full switching time = .36 μs
Peaking time = .14μs

Mechanical: O.D. = .05"
I.D. = .03"
Height = .015"

3.4 Sense Signal, Tolerance and Derivation of the Strobe

Experimental results have indicated that the sense signal is subject to variation in the following ways:

1) Peak amplitude variation : ±50% of nominal
2) Heating effects of both switch and storage cores may shift the time of peak amplitude to about 100 mμs earlier than the room temperature case.
3) Rise time tolerance of X-Y drivers may add ±50 mμs of variation to the time of sense signal peak relative to the X-Y driver turn-on signal.
4) Differences observed in the time of occurrence of the sense signal peak among the 104 cores of a word is 50 mμs.
5) Although no experimental evidence has yet been accumulated, it is expected that the variation in sense signal peak due to position of a word will be negligible. This is a result of the manner in which the sense amplifiers are attached.

The sense signal has a nominal width of 300 mμs which can be shorter, especially at high temperatures when both H_0 decreases and the total flux delivered by the switch decreases. In any case, it appears that the sense signal has an amplitude close to the peak value throughout a 100 mμs interval at least. Hence, we have, in summary, the following conditions for the sense signal:

Amplitude (directly across ends of sense wire): ±75 to ±225 mv
Time of Peak (relative to X-Y driver input): 200 to 400 mμs
Minimum "Width" of Peak: 100 mμs
Maximum Time Tolerance of Signal from cores of the same word: ±50 mμs

Let us consider that the strobe signal brackets the full range of variation of the sense peak and, also, that the binary signal which is recognized corresponds to the polarity existing at the time of strobe turn-off. Then, it can be seen that for sense signals occurring early in the memory cycle, it is possible to recognize the noise which may exist after the sense signal has disappeared (see Figure 13). The maximum noise amplitude to be expected at this

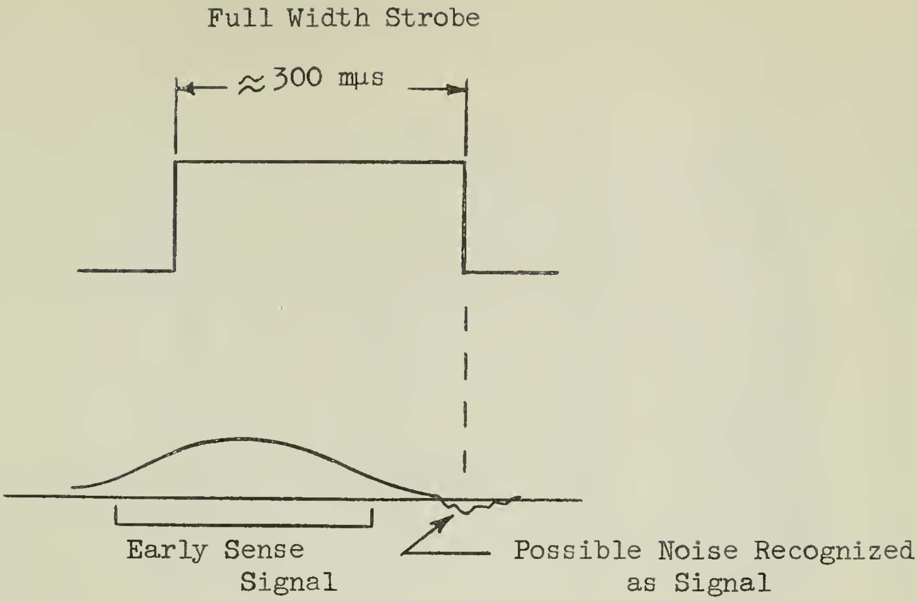


Figure 13

Recognition of Noise as Signal

critical time cannot be accurately determined with the experimental equipment presently in use. It is expected that difficulty may arise from this noise if a fixed strobe is used. Therefore, the possibility of automatic adjustment of the strobe location has been considered. Since the location of the sense peak is largely determined by switch core heating, it is necessary to drive the strobe location by some measure of the condition of the individual word being addressed.

The most straightforward method for accomplishing this appears to be based on the addition of 2 bits per word, one of which exists in the "0" state, the other in the "1" state, in all words. The strobe would then be timed relative to the coincidence of the "0" and "1" signals which are amplified by specialized sense amplifiers having controlled gain.

3.5 Actual Memory Cycle

A diagram showing the nominal timing of the principal events occurring in one memory cycle is given in Figure 14. It can be seen that although the major operations are complete at the 1.2 μs mark, the "cycle end" occurs only at the 1.5 to 2 μs point in order to allow time for settling of the digit lines.

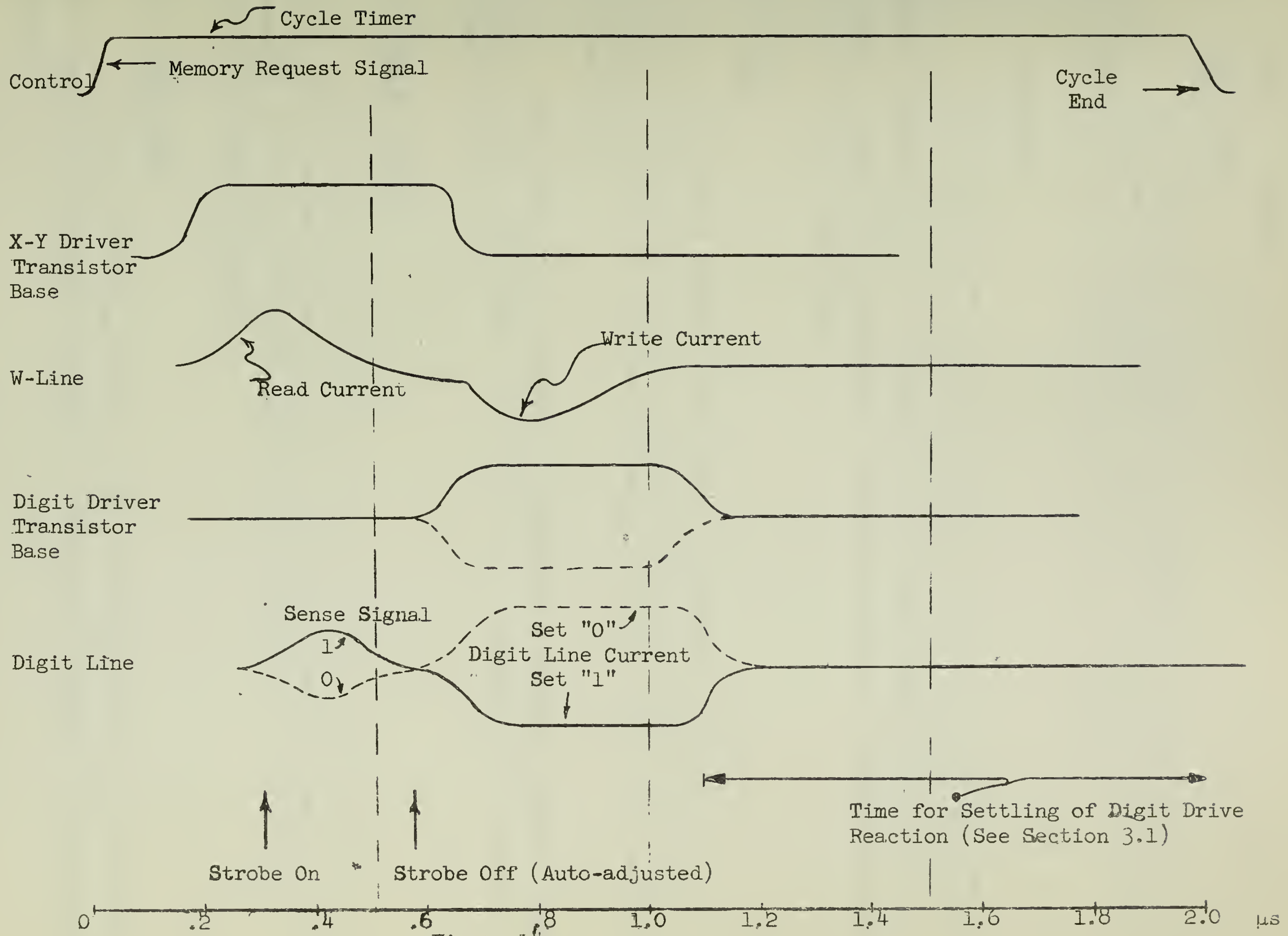


Figure 14
Actual (Nominal) Memory Cycle

4. STATUS OF HARDWARE

4.1 Digit Driver

The digit driver of Figure 15 is accompanied by sufficient data to describe its important characteristics. This form of driver has been operated for several hundred hours. Some minor alterations may be undertaken.

4.2 X-Y Driver

The present X and Y driver is given in Figure 16. The exact design shown differs only slightly from types which have been successfully used for several hundred hours. It is expected that the type 2N560 transistor will be changed to another type having lower saturation resistance in order to further reduce the turn-on delay time.

4.3 Timer

The general design of the timer is illustrated by Figure 17. The use of delay lines is dictated by the desire to maintain the width of the timed output within about ±5% for all component tolerances, including unit-to-unit variations in transistors.

Data given on the diagram will describe the pertinent characteristics. Timers for other pulse lengths will be provided by suitable addition or removal of delay sections.

4.4 Sense Amplifier

The sense amplifier of Figure 18 was designed to meet specifications which existed several months ago. More recently sense amplifier designs to take advantage of the error-detection possibilities afforded by a 2-core-per-bit system have been considered.

4.5 Other Items

The only remaining hardware, used in the memory alone, is the decoder which has not been designed but which is, relatively speaking, a straightforward matter.

Some minor items of specialized nature may be required in connection with strobe derivation and error detection. These may amount to combinations of basic circuits or slight modifications of other memory circuitry.

The remaining hardware will be constructed from the basic circuits.

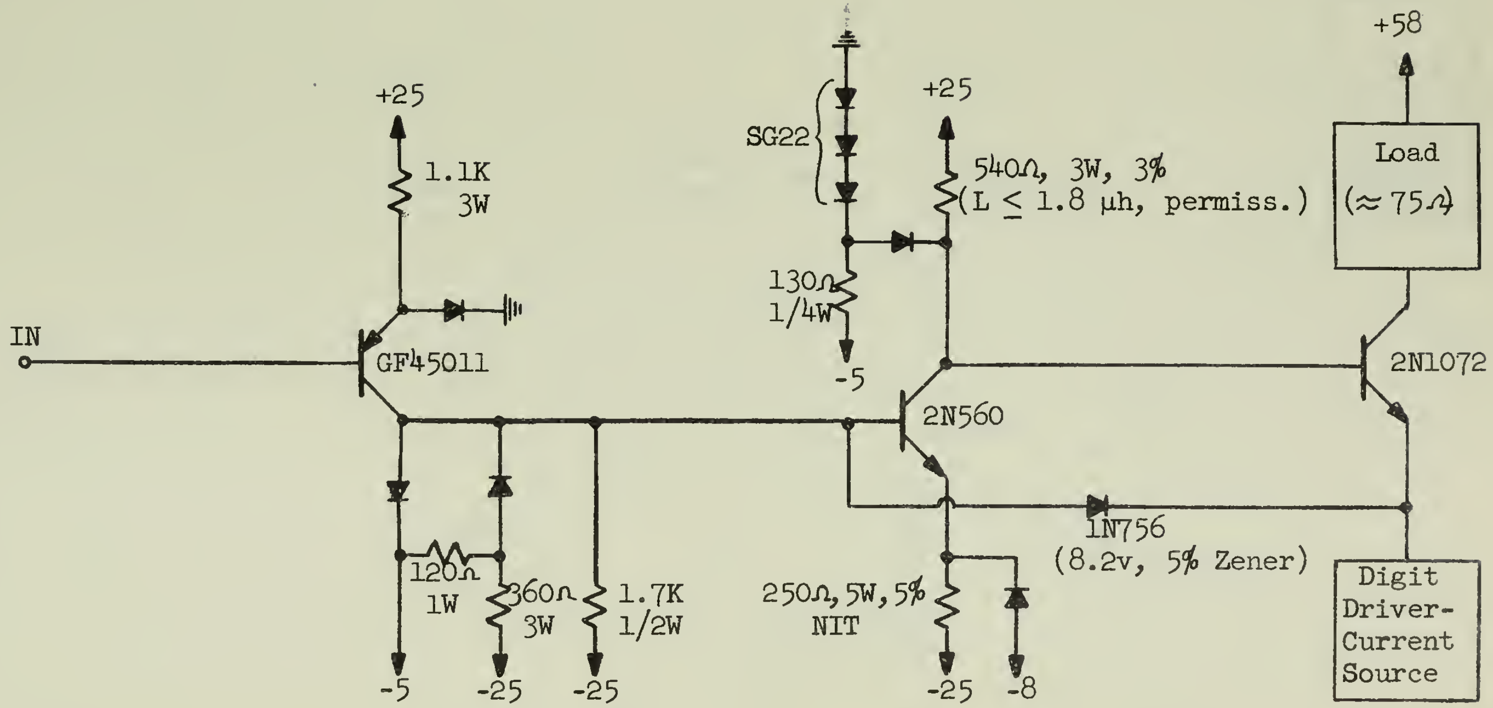


Figure 15

Digit Driver

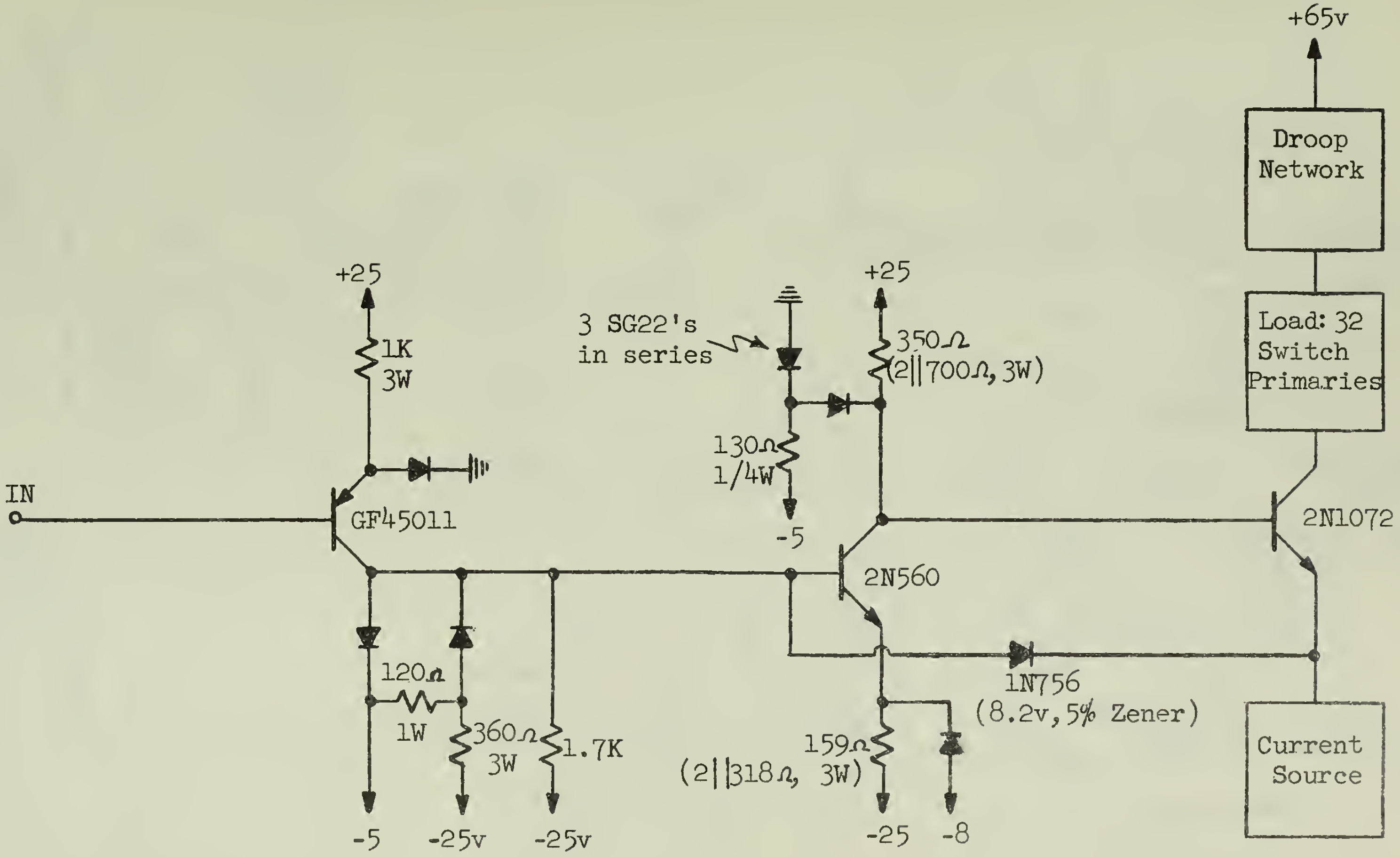
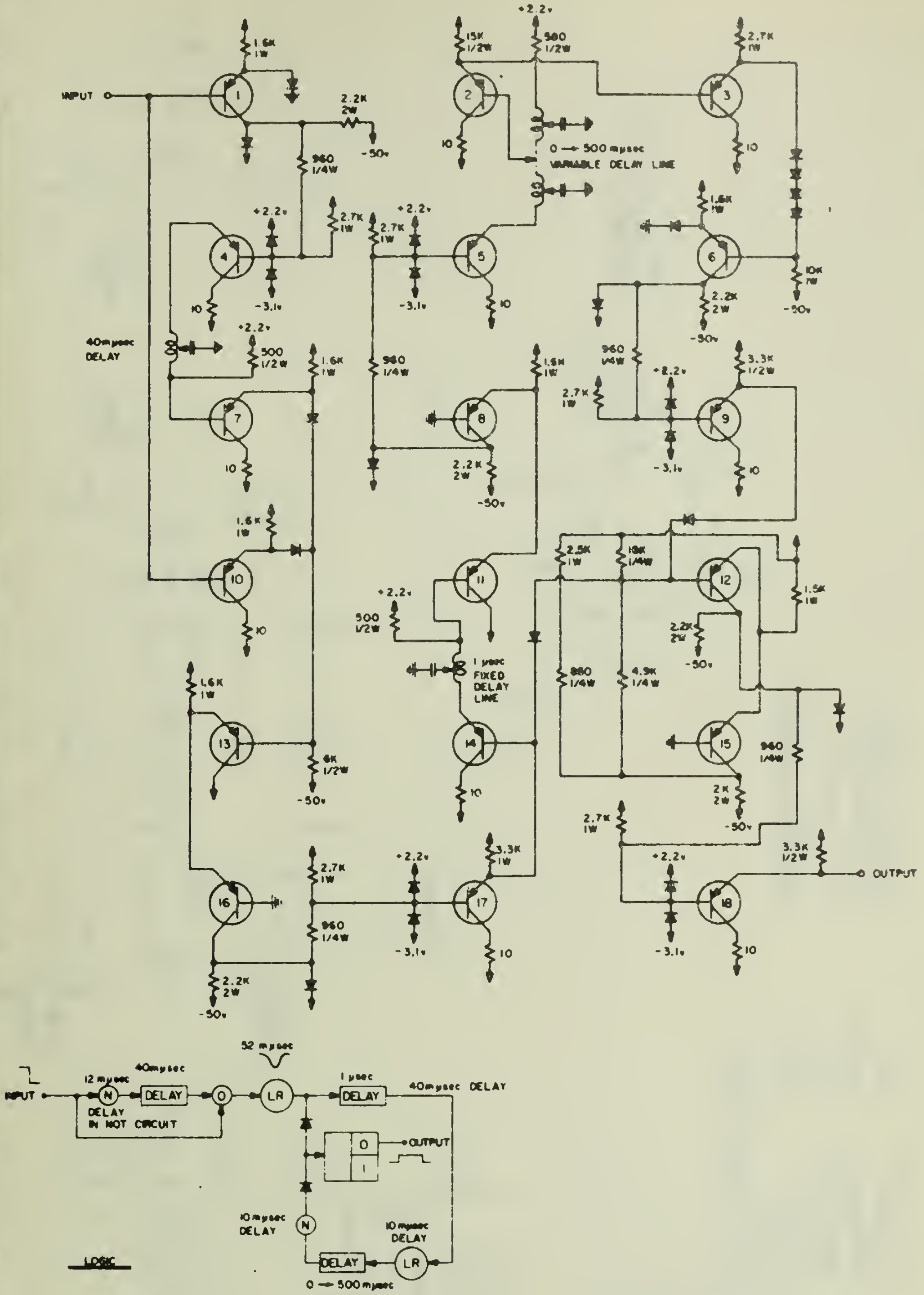


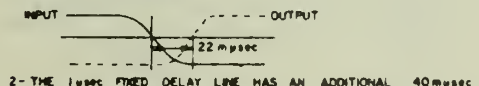
Figure 16

X or Y Driver



NOTES:

1- 22 mμsec DELAY BETWEEN INPUT AND OUTPUT PULSES DUE TO COLLECTOR DELAYS



2- THE 1 μsec FIXED DELAY LINE HAS AN ADDITIONAL 40 mμsec DELAY DUE TO SLOWER RISE TIME AT OUTPUT. ADDITIONAL COLLECTOR DELAYS ALLOW OUTPUT VARIATION OF 1060 to 1580 mμsec.

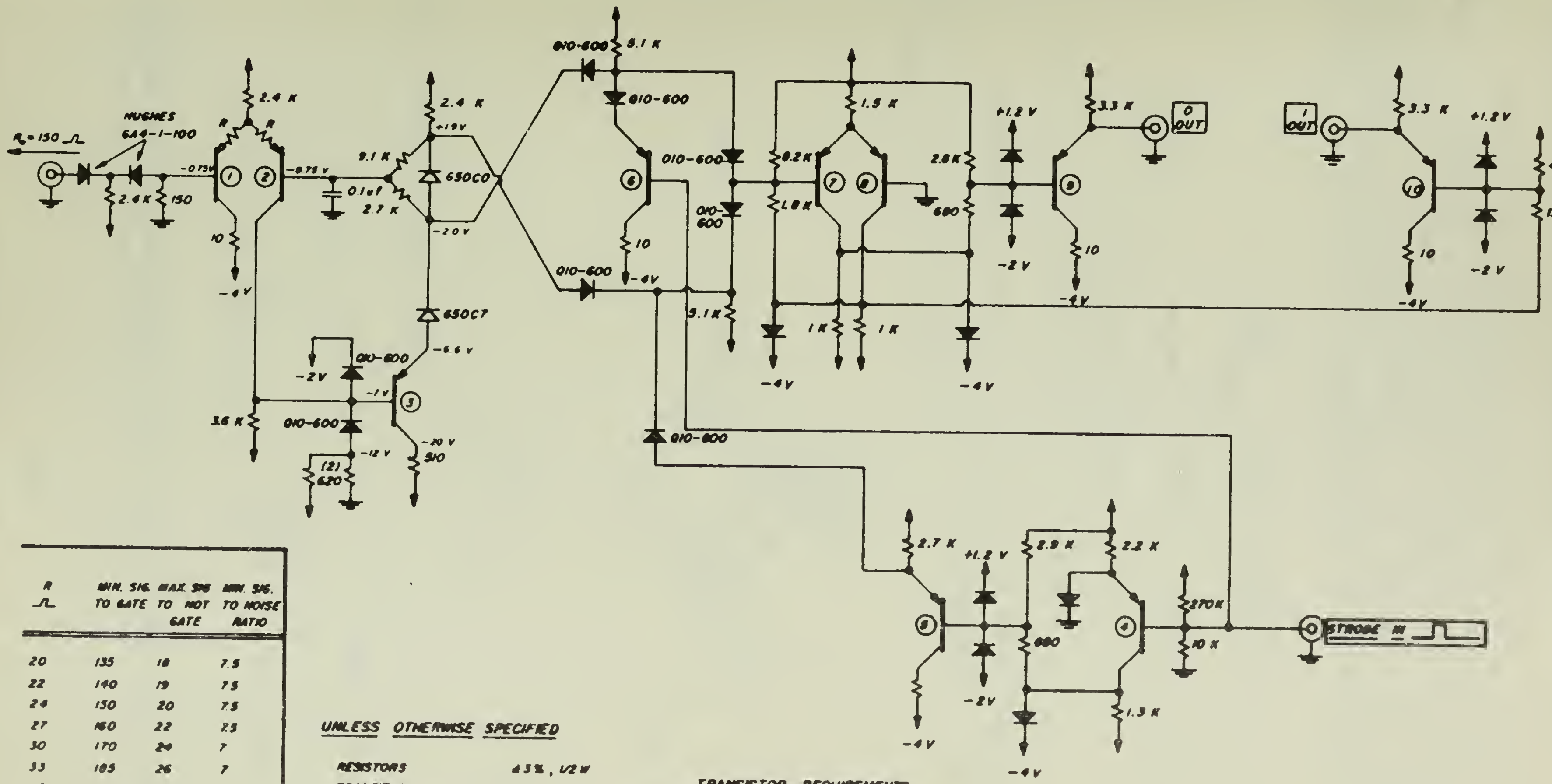
WHEN NOT SPECIFIED

UP VOLTAGE +25v
DOWN VOLTAGE -5v
POWER SUPPLIES ±3%
RESISTORS ±1% 1/2W
ALL 10Ω RESISTORS 1/10W ±10%
DIODES S-577G (SEE DW'G S-654)
TRANSISTORS GF 45011 0.93 [illegible]
(SEE DW'G S-844)

UNIVERSITY of ILLINOIS — GRADUATE COLLEGE — DIGITAL COMPUTER
FOR [illegible] BY J.O. CHECKED [illegible] APPROVED APPROVED J.E. Robertson DATE 8-19-59
TITLE — 1 → 1.5 μsec MEMORY TIMER
IM-88

Figure 17

PRINTED AUG 21 1959



R Ω	MIN. SIG. TO GATE	MAX. SIG TO NOT GATE	MIN. SIG. TO NOISE RATIO
20	135	18	7.5
22	140	19	7.5
24	150	20	7.5
27	160	22	7.5
30	170	24	7
33	185	26	7
36	200	28	7
39	210	30	7
43	220	32	7
47	240	34	7
51	260	36	7
56	290	39	7
62	300	42	7
68	320	45	7
75	350	48	7.5
82	390	51	7.5
91	420	54	8
100	460	56	8
110	500	59	8.5

UNLESS OTHERWISE SPECIFIED

RESISTORS	±5%, 1/2 W
TRANSITORS	GF45011
COLLECTOR DIODES	010-600
OTHER DIODES	05-250
ZENER DIODES	TEXAS INST.
UP VOLTAGES	+25 V
DOWN VOLTAGES	-25 V

TRANSISTOR REQUIREMENTS

1,2,& 3 — $0.96 \leq \alpha \leq 0.98$
AT 5 ma — $5\Omega \leq h_{ib} \leq 15\Omega$
AND OTHERWISE STANDARD
ALL OTHERS — STANDARD

Figure 18

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FOR S.H.L. BY J.E.R. CHECKED S. L. [illegible] APPROVED J.E. Robertson DATE MAR. 31, 1959
TITLE — MEMORY READ AMPLIFIER
M-774

5. APPENDIX--CALCULATIONS CONCERNING THE MAGNETIC SWITCH

Let us first consider the switch and its action as a saturable transformer. An estimate of the current which will be delivered can be made on the basis of the domain-wall motion model of Menyuk and Goodenough[1] using the switching equation derived by Haynes[2]. According to this model, the peak voltage drop across the winding of a switching core for a rectangular applied field is:

$$\frac{d\phi}{dt}_{peak} = v_p = 3.88 \frac{H_n}{S_w} \phi_r$$

where H_n = net magnetic intensity (assumed constant for $t > 0$)

S_w = switching constant

ϕ_r = remanent flux of the core

Considering a switch as in Figure 19 being driven by an mmf $F_1 = N_1 I_1$, biased back by an mmf $F_B = N_B I_B$ and driving a constant resistive load R_2, the following analysis can be made.

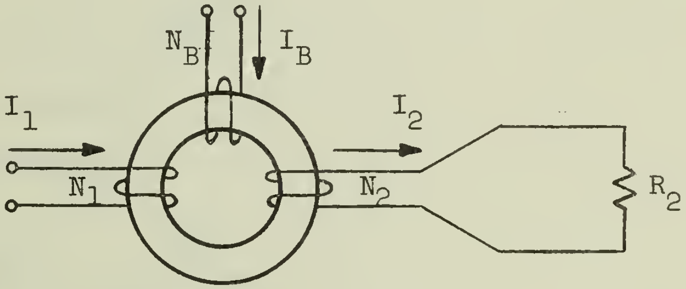

Figure 19

Magnetic Switch

Let F_0 = threshold mmf. Then,

1) $H_n = \frac{1}{d}(F_1 - F_B - F_0 - F_2)$, d = average length of paths around core.

2) $v_{2_p} = N_2 (\frac{d\phi}{dt})_{peak} = N_2 \frac{(3.88 H_n)}{S_w} \phi_r$ (assuming no flux leakage).

---

[1] Menyuk, N. and Goodenough, J.B., Jour. of Appl. Phys., 26:8, 1955.

[2] Haynes, M.K., Jour. of Appl. Phys., 29:3, 1958.

Thus, dividing 2) by R_2 and introducing 1):

$$\frac{v_{2_p}}{R_2} = I_{2_p} = \frac{N_2}{R_2} \frac{3.88}{S_w} \phi_r \frac{1}{d} (F_1 - F_B - F_0 - F_2) ,$$

which, after setting $F_2 = N_2 I_2$, $F_n = F_1 - F_B - F_0$ finally yields:

$$\frac{I_{2_p}}{F_n} = \frac{N_2}{N_2^2 + \frac{dS_w}{3.88\phi_r} R_2} .$$

The above quantity has been called the "transfer ratio"[3]. Here we obtain theoretically a value (viz. $\frac{3.88\phi_r}{dS_w}$) for the r_0 of Raffel.

In the present case, we have:

$$d = .518 \cdot 10^{-2} \text{ m}$$

$$S_w = .6 \cdot 10^{-4} \frac{\text{a-t-sec}}{\text{m}}$$

$$\phi = .6 \ \mu\text{webers}$$

so that the above formula becomes:

$$\frac{I_{2_p}}{F_n} = \frac{N_2}{N_2^2 + \frac{R_2}{7.49}} .$$

For values of R_2 in the range 7-10 Ω , it is easily shown that $N_2 = 1$ turn corresponds to the maximum transfer ratio. If the rise time of driving mmf is short compared to the switching time, presumably the foregoing formula would be a good estiamte. It has been found to be accurate to about 10% in the limited number of cases tried. However, in the case of partial switching, it is likely that the switch core flux becomes exhausted so quickly that the rise time of the drive mmf is a considerable fraction of the switching time, in which case the

---

[3] Raffel, J.I., Switch for Register Selection in a Magnetic-Core Memory, Report R-234, p. 32, Division 6, Lincoln Laboratories, Mass. Inst. of Tech., May 24, 1954.

formula would not be expected to apply. There may also be appreciable effect from the reversible component of switch core flux. Nevertheless, the value of N_2 empirically arrived at agrees with the calculated value.

The windings of the switch core have been chosen as follows by empirical means:

N_x = 2 turns (X Drive line)
N_y = 2 turns (Y Drive line)
N_B = 1 turn (Bias line)
N_w = 1 turn (output or word line) (corresponding to N_2 above).

The latter value verifies the theoretical value for $R_2 = 10\,\Omega$ which is the average effective resistance of a W-line.

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